What is claimed is:

1. A circuit comprising:

a measuring path for receiving a reference signal to sample a pulse to obtain a measured delay;

a forward path connected to the measuring path for delaying the reference signal based on the measured delay to generate an internal signal; and

a feedback path connected to the measuring path and the forward path, the feedback path including a calibrating unit for generating the pulse based on a plurality of feedback signals generated from the reference signal, wherein the calibrating unit is configured to conditionally adjust a pulse width of the pulse.

2. The circuit of claim 1, wherein the calibrating unit includes a selectable delay segment for delaying the reference signal to generate a first feedback signal of the plurality of feedback signals.

3. The circuit of claim 2, wherein the calibrating unit further includes a model delay segment for generating a second feedback signal of the plurality of feedback signals.

4. The circuit of claim 3, wherein the selectable delay segment includes a chain of delay elements.

5. The circuit of claim 4, wherein the model delay segment includes a chain of delay elements.

6. The circuit of claim 3, wherein the calibrating unit further includes a generator connected to the selectable delay segment and the model delay segment for generating the pulse based on the first and second feedback signals.

7. The circuit of claim 1, wherein the measuring path includes a monitoring unit for enabling the calibrating unit to adjust the pulse width of the pulse.

8. The circuit of claim 7, wherein the measuring path further includes a measuring unit for propagating the pulse.

9. The circuit of claim 8, wherein the monitoring unit is configured to reset the measuring unit when the pulse width is adjusted.

10. A circuit comprising:

a calibrating unit for generating a pulse;

a measuring unit for receiving a reference signal to perform a measurement based on a propagation of the pulse within the measuring unit;

a monitoring unit connected to the measuring unit for monitoring the measurement to conditionally enable the calibrating unit to adjust a pulse width of the pulse;

a controller connected to the measuring unit for obtaining a measured delay based on the measurement; and

a main delay unit connected to the controller for receiving the reference signal to generate an internal signal based on the measured delay.

11. The circuit of claim 10, wherein the calibrating unit includes a selectable delay segment for receiving a version of the reference signal to provide a first feedback signal.

12. The circuit of claim 11, wherein the calibrating unit further includes a model delay segment for receiving the version of the reference signal to provide a second feedback signal.

13. The circuit of claim 12, wherein the calibrating unit further includes a generator connected to the selectable delay segment for generating the pulse based on the first and second feedback signals.

14. The circuit of claim 10, wherein the monitoring unit is configured to enable the calibrating unit to increase the pulse width of the pulse.

15. The circuit of claim 14, wherein the monitoring unit is configured to reset the measuring unit when the pulse width is increased.

16. The circuit of claim 10 further including a selector configured to select between the reference signal and a signal at an output node of the main delay unit based on a select signal from the controller.

17. The circuit of claim 10, wherein the calibrating unit includes:

a first delay chain for delaying the reference signal to provide multiple selectable signals;

a selector connected to the first delay chain for selecting among the multiple selectable signals to provide a first feedback signal;

a second delay chain for delaying the reference signal to provide a second feedback signal; and

a generator connected to the second delay chain and the selector to generate the pulse based on the first and second feedback signals.

18. The circuit of claim 17, wherein the selector includes a storage for storing a value.

19. The memory device of claim 18, wherein the selector further includes a number of switches connected to the storage.

20. The circuit of claim 19, wherein the storage includes a shift register.

21. A memory device comprising:

a memory array for storing data;

an output data path for outputting the data; and

a delay lock circuit connected to the data path for providing an internal signal to control a transfer of data at the output data path, the delay lock circuit including:

a measuring path for receiving a reference signal to sample a pulse to obtain a measured delay;

a forward path connected to the measuring path for delaying the reference signal based on the measured delay to generate the internal signal; and

a feedback path connected to the measuring path and the forward path, the feedback path including a calibrating unit for generating the pulse based on a plurality of feedback signals generated from the reference signal, wherein the calibrating unit is configured to conditionally adjust a pulse width of the pulse.

22. The memory device of claim 21, wherein the calibrating unit includes a selectable delay segment for delaying the reference signal to generate a first feedback signal of the plurality of feedback signals.

23. The memory device of claim 22, wherein the calibrating unit further includes a model delay segment for generating a second feedback signal of the plurality of feedback signals.

24. The memory device of claim 23, wherein the calibrating unit further includes a generator connected to the selectable delay segment and the model delay segment for generating the pulse based on the first and second feedback signals.

25. The memory device of claim 24, wherein the selectable delay segment includes a chain of delay elements.

26. The memory device of claim 25, wherein the model delay segment includes a chain of delay elements.

27. The memory device of claim 21, wherein the measuring path includes a monitoring unit for enabling the calibrating unit to adjust the pulse width of the pulse.

28. The memory device of claim 27, wherein the measuring path further includes a measuring unit for propagating the pulse.

29. The memory device of claim 28, wherein the monitoring unit is configured to reset the measuring unit when the pulse width is adjusted.

30. A memory device comprising:

a memory array for storing data;

an output data path for outputting the data; and

a delay lock circuit connected to the data path for providing an internal signal to control a transfer of data at the output data path, the delay lock circuit including:

a calibrating unit for generating a pulse;

a measuring unit for receiving a reference signal to perform a measurement based on a propagation of the pulse within the measuring unit;

a monitoring unit connected to the measuring unit for monitoring the measurement to conditionally enable the calibrating unit to adjust a pulse width of the pulse;

a controller connected to the measuring unit for obtaining a measured delay based on the measurement; and

a main delay unit connected to the controller for receiving the reference signal to generate an internal signal based on the measured delay.

31. The memory device of claim 30, wherein the calibrating unit includes a selectable delay segment for receiving a version of the reference signal to provide a first feedback signal.

32. The memory device of claim 31, wherein the calibrating unit further includes a model delay segment for receiving the version of the reference signal to provide a second feedback signal.

33. The memory device of claim 32, wherein the calibrating unit further includes a generator connected to the selectable delay segment for generating the pulse based on the first and second feedback signals.

34. The memory device of claim 33, wherein the monitoring unit is configured to enable the calibrating unit to decrease the pulse width of the pulse.

35. The memory device of claim 34, wherein the monitoring unit is configured to reset the measuring unit when the pulse width is decreased.

36. The memory device of claim 30 further including a multiplexer configured to select between the reference signal and a signal at an output node of the main delay unit based on a control signal from the controller.

37. The memory device of claim 30, wherein the calibrating unit includes:

a first delay chain for delaying the reference signal to provide multiple selectable signals;

a selector connected to the first delay chain for selecting among the multiple selectable signals to provide a first feedback signal;

a second delay chain for delaying the reference signal to provide a second feedback signal; and

a generator connected to the second delay chain and the selector to generate the pulse based on the first and second feedback signals.

38. The memory device of claim 37, wherein the selector includes a shift register for storing a value.

39. The memory device of claim 38, wherein the selector further includes a number of switches connected to the shift register.

40. A memory device comprising:

a memory array for storing data;

an output data path for outputting the data; and

a delay lock circuit connected to the data path for providing an internal signal to control a transfer of data at the output data path, the delay lock circuit including:

a first chain delay elements located in a first path;

a second chain of delay elements located in a second path;

a third chain of delay elements connected to the first and second paths;

a fourth chain of delay elements connected to the first and second paths;

a selector connected to a subset of delay elements of the third chain; and

a generator connected to the selector, the fourth chain of delay elements, and the first path.

41. The memory device of claim 40, wherein the selector including:

a number of switches connected to the subset of delay elements; and

a storage connected to the switches.

42. The memory device of claim 41, wherein the storage includes a shift register.

43. The memory device of claim 40, wherein the subset of delay elements includes multiple output nodes for providing multiple feedback signals.

44. The memory device of 40, wherein the selector includes a register for storing a value, and wherein the generator is configured to generate a pulse having a pulse width based on the value stored in the register.

45. A system comprising:

a processor; and

a memory device connected to the processor, the memory device including:

a memory array for storing data;

an output data path for outputting the data; and

a delay lock circuit connected to the data path for providing an internal signal to control a transfer of data at the output data path, the delay lock circuit including:

a measuring path for receiving a reference signal to sample a pulse to obtain a measured delay;

a forward path connected to the measuring path for delaying the reference signal based on the measured delay to generate the internal signal; and

a feedback path connected to the measuring path and the forward path, the feedback path including a calibrating unit for generating the pulse based on a plurality of feedback signals generated from the reference signal, wherein the calibrating unit is configured to conditionally adjust a pulse width of the pulse.

46. The system of claim 45, wherein the calibrating unit includes a selectable delay segment for delaying the reference signal to generate a first feedback signal of the plurality of feedback signals.

47. The system of claim 46, wherein the calibrating unit further includes a model delay segment for generating a second feedback signal of the plurality of feedback signals.

48. The system of claim 47, wherein each of the selectable delay segment and the model delay segment includes a chain of delay elements.

49. The system of claim 47, wherein the calibrating unit further includes a generator connected to the selectable delay segment and the model delay segment for generating the pulse based on the first and second feedback signals.

50. The system of claim 45, wherein the measuring path includes a monitoring unit for enabling the calibrating unit to adjust the pulse width of the pulse.

51. The system of claim 50, wherein the measuring path further includes a measuring unit for propagating the pulse.

52. The system of claim 51, wherein the monitoring unit is configured to reset the measuring unit when the pulse width is adjusted.

53. A method comprising:

generating a pulse with an initial pulse width;

sampling the pulse with a reference signal in an initial measurement to obtain a measured delay;

conditionally adjusting the initial pulse width; and

delaying the reference signal based on the measured delay to generate an internal signal.

54. The method of claim 53, wherein generating the pulse includes:

delaying the reference signal to generate a first feedback signal and a second feedback signal, the first and second feedback signals having different timing relationships with each other;

generating a first edge of the pulse using the first feedback signal; and

generating a second edge of the pulse using the second feedback signal.

55. The method of claim 53, wherein conditionally adjusting the pulse includes:

generating a second pulse with a pulse width greater than the initial pulse width if the measured delay is not obtained in the initial measurement; and

sampling the second pulse with the reference signal in a second measurement to obtain the measured delay if the measured delay is not obtained in the initial measurement.

56. The method of claim 53, wherein conditionally adjusting the initial pulse width includes increasing the initial pulse width.

57. The method of claim 53, wherein conditionally adjusting the initial pulse width includes decreasing the initial pulse width.

58. The method of claim 53, wherein generating the pulse includes:

delaying a version of the reference signal using a first delay chain to provide a first feedback signal and using a second delay chain to provide a second feedback signal; and

generating edges of the pulse based on the first and second feedback signals.

59. The method of claim 58, wherein generating the pulse further includes generating a falling edge of the pulse corresponding to a rising edge of the first feedback signal.